



STN3PF06

P-channel 60V - 0.18Ω - 2.5A - SOT-223
STripFET™ II Power MOSFET

PRELIMINARY DATA

Features

Type	V _{DSS}	R _{DS(on)}	I _D
STN3PF06	60V	< 0.20Ω	2.5A

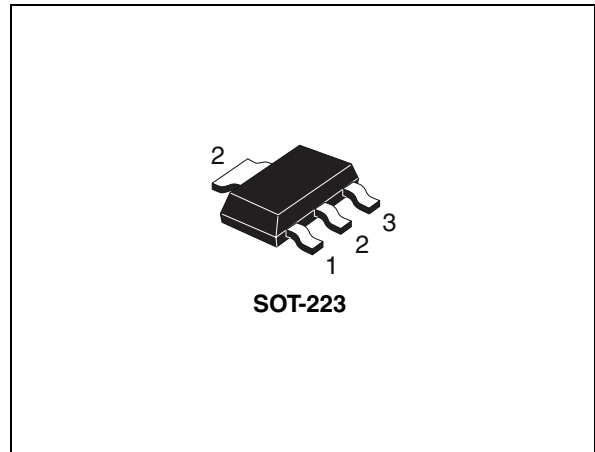
- Extremely dv/dt capability
- 100% avalanche tested
- Application oriented characterization

Description

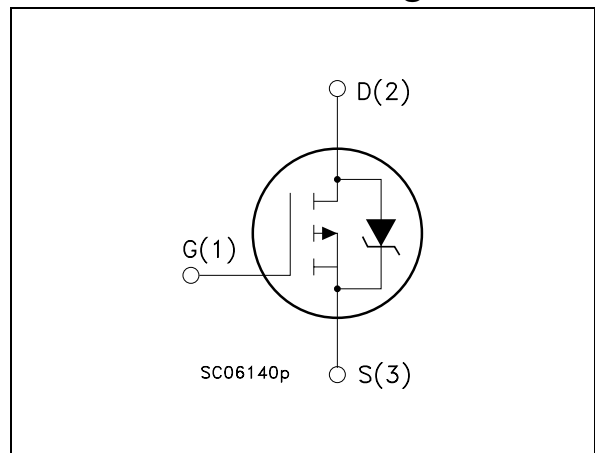
This Power MOSFET is the latest development of STMicroelectronics unique “Single feature size™” strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

Application

- Switching application



Internal schematic diagram



Order code

Part number	Marking	Package	Packaging
STN3PF06	N3PF06	SOT-223	Tape & reel

Note: For the p-channel Power MOSFET actual polarity of voltages and current has to be reversed

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	60	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at $T_C = 25^\circ\text{C}$	2.5	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	1.5	A
$I_{DM}^{(1)}$	Drain current (pulsed)	10	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	2.5	W
	Derating factor	0.02	W/ $^\circ\text{C}$
$dv/dt^{(2)}$	Peak diode recovery voltage slope	6	V/ns
T_j	Operating junction temperature	-65 to 175	$^\circ\text{C}$
T_{stg}	Storage temperature		

1. Pulse width limited by safe operating area

2. $I_{SD} \leq 3\text{A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD} = 80\% V_{(BR)DSS}$

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-pcb}$	Thermal resistance junction-pcb board max	50	$^\circ\text{C}/\text{W}$
R_{thj-a}	Thermal resistance junction-ambient max ⁽¹⁾	60	$^\circ\text{C}/\text{W}$
T_l	Maximum lead temperature for soldering purpose	260	$^\circ\text{C}$

1. Surface mounted

Note: For the p-channel Power MOSFET actual polarity of voltages and current has to be reversed

2 Electrical characteristics

($T_{CASE}=25^{\circ}C$ unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\mu A, V_{GS} = 0$	60			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating}, T_C=125^{\circ}C$			1 10	μA μA
$I_{D(on)}$	On state drain current	$V_{DS} > I_{D(on)} \times R_{DS(on)max},$ $V_{GS} = 10V$	2.5			A
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20V$			± 100	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	2		4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10V, I_D = 40A$		0.18	0.20	Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs}	Forward transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max},$ $I_D = 1.25A$		1.5		S
C_{iss}	Input capacitance	$V_{DS} = 25V, f = 1MHz,$ $V_{GS} = 0$		850		pF
C_{oss}	Output capacitance			230		pF
C_{rss}	Reverse transfer capacitance			75		pF
Q_g	Total gate charge	$I_D = 12A, V_{DD} = 48V,$ $V_{GS} = 10V$ <i>(see Figure 2)</i>		16	21	nC
Q_{gs}	Gate-source charge			4		nC
Q_{gd}	Gate-drain charge			6		nC

Note: For the p-channel Power MOSFET actual polarity of voltages and current has to be reversed

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	$V_{DD}=30V$, $I_D=6A$, $R_G=4.7\Omega$, $V_{GS}=10V$ (see Figure 1)		20 40		ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time	$V_{DD}=30V$, $I_D=6A$, $R_G=4.7\Omega$, $V_{GS}=10V$ (see Figure 1)		40 10		ns ns
$t_{r(Voff)}$ t_f t_c	Off-voltage rise time Fall time Cross-over time	$V_{clamp}=48V$, $I_D=12A$, $R_G=4.7\Omega$, $V_{GS}=10V$ (see Figure 1)		10 17 30		ns ns ns

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current				2.5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				10	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 2.5A$, $V_{GS} = 0$			1.2	V
t_{rr}	Reverse recovery time	$I_{SD} = 12A$, $di/dt = 100A/\mu s$ $V_{DD} = 30V$, $T_j = 150^\circ C$		100		ns
Q_{rr}	Reverse recovery charge			260		μC
I_{RRM}	Reverse recovery current			5.2		A

1. Pulse width limited by T_{jmax}

2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Note: For the p-channel Power MOSFET actual polarity of voltages and current has to be reversed

3 Test circuit

Figure 1. Switching times test circuit for resistive load

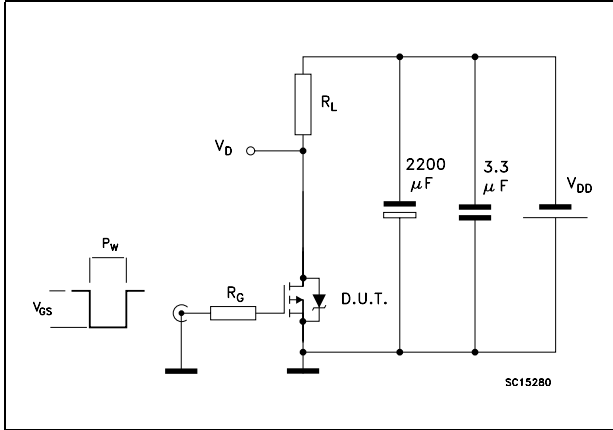


Figure 2. Gate charge test circuit

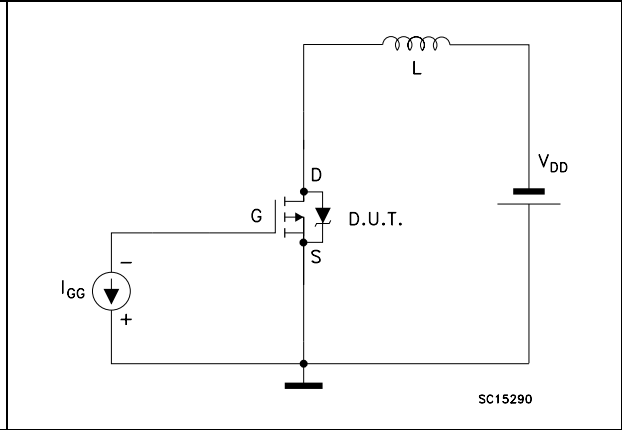
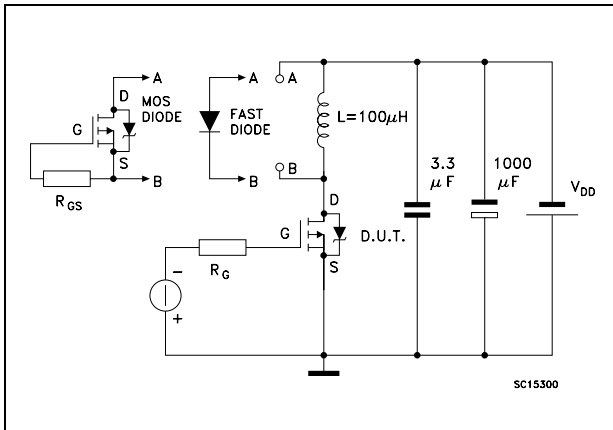


Figure 3. Test circuit for inductive load switching and diode recovery times

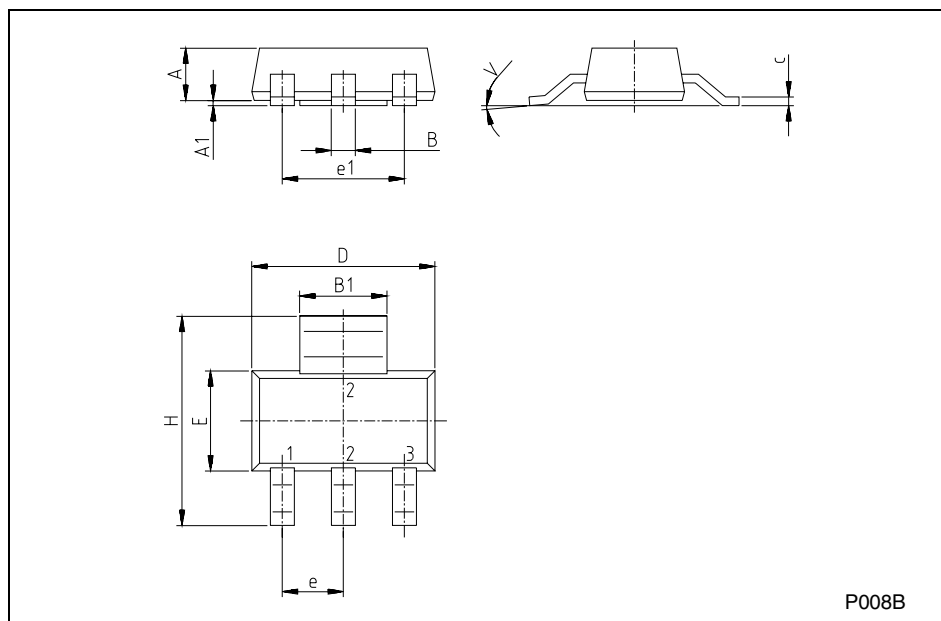


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

SOT-223 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.80			0.071
B	0.60	0.70	0.80	0.024	0.027	0.031
B1	2.90	3.00	3.10	0.114	0.118	0.122
c	0.24	0.26	0.32	0.009	0.010	0.013
D	6.30	6.50	6.70	0.248	0.256	0.264
e		2.30			0.090	
e1		4.60			0.181	
E	3.30	3.50	3.70	0.130	0.138	0.146
H	6.70	7.00	7.30	0.264	0.276	0.287
V			10°			10°
A1		0.02				



5 Revision history

Table 7. Revision history

Date	Revision	Changes
08-May-2007	3	The document has been reformatted

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